Reg. No ..... Name **23U352**

END SEMESTER EXAMINATION : NOVEMBER 2023

SEMESTER 3 : INTEGRATED M.Sc. PROGRAMME COMPUTER SCIENCE

COURSE : **21UP3CRMCP10 : COMPUTER ORGANIZATION AND ARCHITECTURE**

(For Regular 2022 Admission and Improvement/Supplementary 2021 Admission)

Time : Three Hours Max. Weightage: 30

PART A

Answer any 8

1. The number of bits in the control word of a CPU architecture with seven general purpose registers is _____.
2. Write the formula to calculate the effective address of an operand.
3. In 2's complement system, the leftmost bit is _____ for negative numbers.
4. List any two examples of cache coherence protocols.
5. If a RAM is of size 128 x 8, calculate the number of bits required as the address bits.
6. The ---------- register points to the top of the stack.
7. State the main advantage of having a modular memory.
8. Define Gray code in number system.
9. In a 16-bit address bus, the --------- bit position indicates the selection of RAM or ROM.
10. The typical access time ratio between cache and main memory is in the range _____.

(1 x 8 = 8 weight)

PART B

Answer any 6

11. With a diagram, explain how memory is connected to CPU.
12. Write short notes on multiprogramming.
13. Consider the expression X = (AB + CD)/E. Write the instructions that evaluates the expression in two-address form.
14. Write brief notes on hypercube connection.
15. List the steps involved in the instruction cycle of an instruction pipeline.
16. With an example, differentiate between register notation and assembly language notation of machine instructions.
17. A computer must have instructions capable of performing four types of operations. List the operations.
18. Multiprocessing can improve performance by decomposing a program into parallel executable tasks. Discuss how this can be acheived.

(2 x 6 = 12 Weight)

PART C
Answer any 2

19. Make short notes on RISC instructions. Write the RISC instructions for the following expression:
    X = (P / Q) x (Q -R)
20. Implement the logic function F = (XZ + Y'Z + X'YZ)' using universal gates alone.
21. Discuss how straight-line sequencing and branching are performed by the CPU.
22. With an example of page replacement, explain the LRU algorithm.

(5 x 2 = 10 weight)